HALDIA INSTITUTE OF TECHNOLOGY

(AN AUTONOMOUS INSTITUTION UNDER MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL)

Paper Code: Computer Organization and Architecture

Paper Name: PCC-CS 402

Time Allotted: 2 Hours *Full Marks*: 70

The figures in the margin indicate full marks
Candidates are required to give their answers in their own words as far as practicable

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives from the followings: 30 x 1 = 30

(i) The spatial aspect of the locality of reference means____ [CO3]

a) That the recently executed instruction is executed again next

b) That the recently executed won't be executed again

c) That the instruction executed will be executed at a later time

d) That the instruction in close proximity of the instruction executed will be executed in future

(ii) In IEEE 32-bit representations, the mantissa of the fraction is said to occupy ____ bits.

a) 24 b) 23 c) 20 d) 16 [CO1]

(iii) The correspondence between the main memory blocks and those in the cache is given by____ [CO3]

a) Hash function b) Mapping function
c) Locale function d) Assign function

(iv) Whenever the data is found in the cache memory it is called as____ [CO3]
a) Hit b) Miss c) Found d) Error

(v) Which of the following circuit is used to store one bit of data? [CO2]
a. Flip Flop b. Decoder c. Encoder d. Register

(vi) In multiple Bus organisation, the registers are collectively placed and referred as _____
a) Set registers b) Register file c) Register Block d) Map registers [CO2]

(vii) In the case of, Zero-address instruction method the operands are stored in _____
a) Registers b) Accumulators c) Push down stack d) Cache [CO4]

(viii) The addressing mode/s, which uses the PC instead of a general purpose register is _____ [CO4]
a) Indexed with offset b) Relative c) Direct d) Both Indexed with offset and direct

(ix) Which method/s of representation of numbers occupies a large amount of memory than others? [CO3]
a) Sign-magnitude b) 1's complement c) 2's complement d) 1's & 2's compliment

(x) When generating physical addresses from a logical address the offset is stored in _____ [CO3]
a) Translation look-aside buffer b) Relocation register c) Page table d) Shift register

(xi) CPU gets the address of next instruction to be processed from [CO1]

a) Instruction register b) Memory address register

c) Index register d) Program counter

(xii) Subtractor can be implemented by [CO2]

a) Adder b) Complementor
c) Both (a) and (b) d) None of these

(xiii) Which of the following techniques used to effectively utilize main memory?
a) Address binding b) Dynamic linking c) Dynamic loading d) Both Dynamic linking and loading [CO3]

(xiv) In a system, which has 32 registers the register id is _____ long.
a) 16 bit b) 8 bits c) 5 bits d) 6 bits [CO2]

(xv)The reason for the cells to lose their state over time is _____ [CO2]
a) Use of Shift registers b) The lower voltage levels
c) Usage of capacitors to store the charge d) None of the mentioned

(xvi) In order to read multiple bytes of a row at the same time, we make use of _____
a) Memory extension b) Cache c) Shift register d) Latch [CO2]

(xvii) The chip can be disabled or cut off from an external connection using _____
a) ACPT b) RESET c) LOCK d) Chip select [CO2]

(xviii) In a 4M-bit chip organization has a total of 19 external connections, and then it has _____ address if 8 data lines are there.
a) 2 b) 5 c) 9 d) 8 [CO3]

(xix) The temporal aspect of the locality of reference means _____ [CO3]
a) That the recently executed instruction won't be executed soon
b) That the recently executed instruction is temporarily not referenced
c) That the recently executed instruction will be executed soon again
d) None of the mentioned

(xx) To reduce the number of external connections required, we make use of _____ [CO2]
a) De-multiplexer b) Multiplexer c) Encoder d) Decoder

(xxi) The block transfer capability of the DRAM is called _____ [CO3]
a) Burst mode b) Block mode c) Fast page mode d) Fast frame mode

(xxii) To get the physical address from the logical address generated by CPU we use _____ [CO3]
a) MAR b) MMU c) Overlays d) TLB

(xxiii) The technique used to store programs larger than the memory is _____ [CO3]
a) Overlays b) Extension registers c) Buffers d) Both Extension registers and Buffers

(xxiv) A 16 X 8 Organization of memory cells, can store up to _____ [CO3]
a) 256 bits b) 1024 bits c) 512 bits d) 128 bits

(xxv) In a 4M-bit chip organization has a total of 19 external connections then it has _____ address if 8 data lines are there. [CO3]
a) 10 b) 8 c) 9 d) 12

(xxvi) Which one of the following is the advantage of virtual memory? [CO3]

a) Faster access to memory on an average b) Process can be given protected address space
c) Program larger than the physical memory can be run d) None of these

(xxvii) The stored program concept is [CO1]

a) The program and data need to be resident in main memory at run time
b) Program cannot be stored in secondary memory
c) No modification of program
d) No use of register in program

(xxviii) The computer architecture aimed at reducing the time of execution of instructions is _____ [CO4]
a) CISC b) RISC c) ISA d) ANNA

(xxix) Pipe-lining is a unique feature of _____ [CO6]
a) RISC b) CISC c) ISA d) IANA

(xxx) Which memory device is generally made of semiconductors? [CO3]
a) RAM b) Hard-disk c) Floppy disk d) Cd disk

Group – B
(Multiple Choice Type Questions)

2. Choose the correct alternatives from the followings: 10 x 2 = 20

(i) Normalized representation of 0.00101×2^2

[CO1]

a) 0.00101×2^2 b) 1.01×2^2 c) 1.01×2^{-1} d) None of these

(ii) Multiply 207.75 and -2.375

a) 1.01111100001*2^3 b) .001111100011*2^6 c) 1.01000001100001*2^9 [CO1]

(iii) Consider a computer which supports 32 2 address instructions. If the address length is 8 bits then the length of the instruction is _____ bits [CO4]

a) 8 b) 21 c) 24 d) 32

(iv) In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____ [CO2]

a) EA = 5+R1 b) EA = R1 c) EA = [R1] d) EA = 5+[R1]

(v) An 24 bit address generates an address space of _____ locations. [CO3]

a) 1024 b) 4096 c) 248 d) 16,777,216

(vi) A memory organization that can hold upto 1024 bits and has a minimum of 10 address lines can be organized into _____ [CO3]

a) 128 X 8 b) 256 X 4 c) 512 X 2 d) 1024 X 1

(vii) In associative mapping, in a 16 bit system the tag field has _____ bits. [CO3]

a) 12 b) 8 c) 9 d) 10

(viii) A processor support a maximum of 4gb where the memory is word addressable. Find the size of the address bus of the processor [CO4]

a) 32 bits b) 31 bits c)34 bits d) 30 bits

(ix) Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster.

a) A b) B c) Both take the same time d) Insufficient information [CO6]

(x) How many 3K X 1 Ram chips are needed to provide a memory capacity of 256 kb.

a) 8 b) 32 c) 64 d) 128 [CO3]

Group – C

(Short Answer Type Questions)

3. Attempt any four from the followings: 4 x 5 = 20

i)Find the value represented by the following 32 bits in IEEE754 representation

01000001111000…00. [CO1]

ii) Perform the arithmetic operation in binary using 2's complement representation
(i). (+42) + (-13) (ii) (-42) – (-13). [CO1]

iii) What are addressing modes? Explain the various addressing modes with examples. [CO4]

iv) A processor has 40 distinct Instructions and 24 general purpose registers. A 32 bit Instruction word has an opcode, two register operands and an intermediate operand. Find the no of bits available for the immediate operand field. [CO4]

v) How many 128*8 RAM chips are needed to provide a memory capacity of 256*16 bits. How many address bus lines must be used to access 256*16 bits of memory and what should be the decoder size for the chip select? [CO3]

vi) Explain about arithmetic pipelining? Define parallel processing and explain the flynn's classification of computer with suitable diagram. [CO6]

Uddalak Chatterjee

Signature of the Paper Setter/Moderator

Answer Key:

Group – A

1. (i) d	(ii) b	(iii) b	(iv) a	(v) a	(vi) b
(vii) c	(viii) b	(ix) a	(x) b	(xi) d	(xii) c
(xiii) c	(xiv) c	(xv) c	(xvi) d	(xvii) d	(xviii) c
(xix) c	(xx) b	(xxi) c	(xxii) b	(xxiii) a	(xxiv) d
(xxv) c	(xxvi) c	(xxvii) a	(xxviii) b	(xxix) a	(xxx) a

Group – B

2. (i) c	(ii) c	(iii) b	(iv) d	(v) d	(vi) d
(vii) a	(viii) b	(ix) a	(x) c		

Group – C

3. (i) (ii) (iii) (iv) (v) (vi)