HALDIA INSTITUTE OF TECHNOLOGY

(AN AUTONOMOUS INSTITUTION UNDER MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL)

Paper Code: PCC-CS 402

Paper Name: Computer Organization and Architecture

Time Allotted: 3 Hours *Full Marks*: 70

The figures in the margin indicate full marks

Candidates are required to give their answers in their own words as far as practicable

Group – A
(Multiple Choice Type Questions)

Choose the correct alternatives from the followings: 15 x 1 = 15

1. (i)In IEEE 32-bit representations, the mantissa of the fraction is said to occupy ____ bits. [CO1]
a) 24 b) 23 c) 20 d) 16

(ii)When signed numbers are used in binary arithmetic, then which one of the following notations would have a unique representation for 0? [CO1]
a) Signed magnitude b) 1's complement c) 2's complement d) None

(iii)Subtractor can be implemented by [CO2]
a) Adder b) Complementor c) Both (a) and (b) d) None of these

(iv)By left-shifting the content of a register once, its content is [CO2]
a) Doubled b) Halved c) Both (a) and (b) d) No such decision can be made

(v)To add two n-bit numbers in a parallel adder, the number of clock periods required is [CO2]
a) 1 b) 2n c) n d) n/2

(vi)If the value V(x) of the target operand is contained in the address field itself, the addressing mode is
a) Immediate b) Direct c) Indirect d) Implied [CO4]

(vii)In a system, which has 32 registers the register id is _____ long. [CO4]
a) 16 bits b) 8 bits c) 5 bits d) 6 bits

(viii)The initial bootstrap program is generally stored in [CO1]
a) RAM b) ROM c) Magnetic Disk d) Cache

(ix)Number of transistors in a CMOS static RAM cell [CO3]
a) 1 b) 4 c) 6 d) None of these

(x)Physical memory broken down into groups of equal size is called [CO3]
a) Page b) Tag c) Block d) Index

(xi)Cache memory is used to increase the speed of [CO3]
a) Hard disk b) CPU c) Floppy disk d) None of these

(xii)An instruction pipeline can be implemented by means of [CO6]
a) LIFO Buffer b) FIFO Buffer c) Stack d) None of these

(xiii)The periods of time when the unit is idle are called _____ [CO6]
a) Stalls b) Bubbles c) Hazards d) Both Stalls and Bubbles

(xiv)Each stage in pipelining should be completed within _____ cycle. [CO5]
a) 1 b) 2 c) 3 d) 4

(xv)Pipe-lining is a unique feature of _____[CO4]
a) RISC b) CISC c) ISA d) IANA

Group – B
(Short Answer Type Questions)

Attempt any three from the followings: 3 x 5 = 15

2. Perform the arithmetic operation in binary using 2's complement representation [CO1]
(i). $(-34) + (-12)$ (ii) $(17) - (35)$ (2.5× 2)

3. What is meant by "instruction set of a machine"? What are the different parameters that determine the design of an instruction set of a machine? Explain. (5) [CO4]

4. What is cache memory? How does cache memory increase the performance of a computer? What is the hit ratio? (5) [CO3]

5. Explain Flynn's classification of computers with a suitable diagram. (5) [CO6]

6. What do you mean by the performance of a computer? What is MIPS? (5) [CO6]

Group – C
(Long Answer Type Questions)

Attempt any four from the followings: 4 x 10 = 40

7. (a) Construct a common Bus using Muxs with four registers n bit each. [CO2]
(b)Design a logic unit that performs four logic operations AND, OR, NAND, and XOR. [CO2] (5+5)

8.(a)What are 0,1,2 and 3 address machines? Give examples. [CO4]
(b)Convert the following expression into three-address, two-address, one-address, and zero-address instruction.
X = (A+B) *C [CO4](3+7)

9. (a)If each register is specified by 3 bits and the instruction ADD R1, R2, R3 is two bytes long; then what is the length of the opcode field? [CO4]
(b)Compare and contrast between CISC and RISC. [CO4] (5+5)

10.(a)Describe the operation of cache memory. What is meant by "the cache memory has a hit ratio of 0.8"? [CO3]
(b)A hierarchical cache-main memory subsystem has the following specifications:
The cache access time of 50 nanoseconds,the main memory access time of 500 nanoseconds,80% of the memory request is for reading,a hit ratio of 0.9 for read access, and the write-through scheme is used. Calculate the following:
i).Find out the average access time of the memory system considering only the memory read cycle. [CO3]
ii).Find out the average access time of the system both for read and write requests. (2+2+3+3)

11. (a)What is Pipelining. What are the speedup, throughput, and efficiency of a pipelined architecture? [CO6]
(b) Deduce that the maximum speed-up in a K-stage pipeline processor can be K. Is this maximum speed-up always achievable? Explain. [CO6] (5+5)

12. (a) What are the instruction pipeline and arithmetic pipeline? [CO6]
(b)What do you mean by pipeline hazards? What are the different types of pipeline hazards? Explain each ofthem. [CO6] (4+6)