HALDIA INSTITUTE OF TECHNOLOGY

(AN AUTONOMOUS INSTITUTION UNDER MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL)

Paper Code: PCC-CS 503

Paper Name: Microprocessor and Microcontroller

Time Allotted: 1 Hours 30 Minutes *Full Marks*: 70

The figures in the margin indicate full marks
Candidates are required to give their answers in their own words as far as practicable

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives from the followings: 30 x 1 = 30

(i) Which signal causes immediate termination of all activities of 8085?

a) RESET Signal b) Interrupt Signal c) Both d) None [CO1]

(ii) Which of the following are the two main important components of CPU?

a) Control Unit and registers b) Registers and main memory c) Control unit and ALU
d) ALU and memory [CO1]

(iii) The number of software interrupt in 8085 is

a) 2 b) 3 c) 8 d) 5 [CO4]

(iv) The maximum number of available ports in 8255 is

a) 2 b) 3 c) 4 d) 6 [CO1]

(v) In 8085 which addressing mode is also called inherent addressing mode

a) Direct b) Register c) Implicit d) Immediate [CO2]

(vi) The number of machine cycles and T states present in DCX instruction of 8085 are

a) 1, 4 b) 2, 4 c) 1, 6 d) 2,6 [CO2]

(vii) The last machine cycle of STAX B instruction in 8085 is

a) Memory write b) memory read c) I/O write d) I/O read [CO2]

(viii) The 2nd machine cycle of instruction ADI 0EH is

a) memory write b) memory read c) I/O read d) I/O write [CO2]

(ix) The longest instruction in 8086 microprocessor is of length

a) 10 Byte b) 6 Byte c) 12 Byte d) 14 Byte [CO2]

(x) _____ flag is affected by DCX instruction in 8085

a) AC b) CY c) Z d) none of these [CO2]

(xi) The status of the flag which cannot be operated by direct instruction is

a) CY b) P c) Z d) AC [CO1]

(xii) Which is used to store critical piece of data during execution of subroutines and interrupts?

a) Stack b) Accumulator c) Data register d) Queue [CO3]

(xiii) The total number of available 16 bit registers in 8257 DMA controller is/are

a) 2 b) 1 c) 8 d) 4 [CO6]

(xiv) Which is not a control bus signal?

a) READ b) WRITE c) RESET d) None

[CO1]

(xv) Each memory location has

a) Address b) Content c) Both a and b d) none

[CO1]

(xvi) Secondary memory can store

a) Program code b) Compiler c) OS d) All of the above [CO5]

(xvii) BIU stands for

a) Bus interface unit b) basic interface unit c) Bath a and b d) none [CO1]

(xviii) EU stands for

a) Execution unit b) Executable unit c) both of the above d) none [CO1]

(xix) Size of each segment in 8086 is

a) 32KB b) 16KB c) 64KB d) 128KB [CO1]

(xx) Registers which are partially available to user during programming in 8085 are called

a) PC b) Memory address registers c) General purpose registers d) Flag register [CO1]

(xxi) A 32-bit address bus allows access to a memory of capacity

64 Mb (b) 16 Mb (c) 1Gb (d) 4 Gb [CO5]

(a)

(xxii) The contents of accumulator before CMA instruction is A5H. Its content after instruction execution is

a) 00H b) A5H c) 5AH d) 00H [CO3]

(xxiii) The number of machine cycles required to execute the following 8085 instructions

(i) LDA 3000H
(ii) LXI D, FOF1H would be

a) 2 for (i) and 2 for (ii) b) 4 for (i) and 3 for (ii) c) 3 for (i) and 3 for (ii) d) 2 for (i) and 4 for (ii) [CO3]

(xxiv) Registers, which are used to hold conditional in 8085, are known as

a) PC b) Memory address registers c) General purpose registers d) Flags [CO1]

(xxv) In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is

a) Non maskable and non vectored b) Maskable and non vectored c) non maskable and vectored d) Maskable and vectored [CO4]

(xxvi) The number on machine cycles in the instruction XCHG is

a) 1 b) 2 c) 3 d) 4 [CO2]

(xxvii) In 8085 microprocessor, RST6 transfers program execution to following location

a) 0030H b) 0042H c) 0024H d) 0060H [CO2]

(xxviii) Assuming HL pair contains 0242H, the instruction DAD H will change the content of HL pair to

a) No change b) 0484H c) 0000H d) 0844H [CO2]

(xxix) Assume register HL pair is cleared and SP contains 2099H, after execution of the instruction DAD SP, the content of HL pair will be

a) 2099H b) 3000H c) 0000H d) No change [CO2]

(xxx) Which is an 8 bit Microprocessor _____

a) Intel 4040 b) 8085 c) Pentium -1
d) 8086 [CO1]

Group – B

(Multiple Choice Type Questions)

2. Choose the correct alternatives from the followings: 20 x 2 = 40

(i) In an 8085 microprocessor, the instruction CMP B has been executed while the contents of accumulator are less than that of register B. As a result carry flag and zero flag will be respectively

a) Set, reset b) reset, set c) reset, reset d) set, set [CO3]

(ii) Taking the clock frequency of 8085 microprocessor to be 2 MHz, the delay generated by the given subroutine is

```
    MVI C, FFH
LOOP DCR C
    JNZ LOOP
```

a) 0.787mSec b) 2.78 mSec c) 0.11 mSec d) 3.78 mSec [CO3]

(iii) In BSR mode of 8255, only port C can be used to

a) Set individual ports b) Reset individual ports c) Set and reset individual ports d) Programmable I/O port [CO6]

(iv) In LDAX instruction of 8085 microprocessor

a) Only Sign flag is affected b) Only AC flag is affected c) Only Zero flag is affected d) None of the above [CO2]

(v) Which operation mode of 8253/54, PIT peripheral generates perfect square wave at the OUT pin

a) Mode 1 b) Mode 2 c) Mode 0 d) Mode 3 [CO6]

(vi) The number of bytes, machine cycles and T states in the instruction LHLD are

a) 1, 5, 12 b) 1, 5, 13 c) 3, 5, 16 d) 3, 5, 18 [CO2]

(vii) In order to change the accumulator content from F6H to 6FH, the number of rotate instructions required will be

a) 4 b) 2 c) 3 d) 8 [CO2]

(viii) Consider the following set of instructions. After execution the content of accumulator will be

```
MVI A, F8H
XRA A
```

a) FFH b) 00H c) 8FH d) F8H [CO3]

(ix) Consider the following set of instructions, after execution by 8085

```
MVI A, 0CH
SIM
```

a) RST 7.5 is masked b) RST 5.5 is masked c) RST 6.5 is masked d) all interrupts are masked [CO3]

(x) In 8086 microprocessor, if the flag content is 0F00H then

a) Overflow flag is set b) Interrupt flag is set c) both flags are set d) both flags are reset [CO2]

(xi) The _____ ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus.

a) Control bus b) Control instruction c) CPU d) Address decoder [CO1]

(xii) To put the 8085 microprocessor in the wait state

a) Lower the HOLD input b) Lower the READY input c) Higher the READY input d) Higher the READY input [CO2]

(xiii) The microprocessor 8085 has _____ basic instructions and _____ opcodes.

a) 74, 246 b) 246, 80 c) 77, 323 d) 78, 245 [CO1]

(xiv) If the following set of instructions is executed by 8085 microprocessor

```
MVIA 33H
MVI B 78H
ADD B
CMA
ANI 32H
```

The content of the accumulator post execution is

a) 00H b) 10H c) 11H d) 32H [CO3]

(xv) Out of the given instructions, one which affects the Accumulator is

a) MOV B,M b) PCHL c) RNZ d) SBI BEH [CO2]

(xvi) After the execution of the following program in 8085 microprocessor

```
MVI A 05H
MVI B 05H
PTR: ADD B
DCR B
JNZ PTR
ADI 03H
HLT
```

The accumulator content will be

a) 17H b) 20H c) 23H d) 05H [CO3]

(xvii) The controlling peripheral which takes control of the buses and transfer data directly between the source and destination without microprocessor intervention is known as

a) DMA Controller b) READ/WRITE Controller c) MASTER/SLAVE Controller d) HGH SPEED Controller [CO6]

(xviii) If the 8085 microprocessor is externally clocked at a frequency of 5 MHz, and execution time of an instruction is 1.6 micro seconds then the instruction has

a) 1 b) 6 c) 4 d) 5 [CO1]

(xix) Execution of following set of instructions will

EI
MVI A 08H
SIM

a) Disable all interrupts b) Enable all interrupts c) Disable RST 7.5 and 6.5 d) Enable RST 7.5 and 6.5 [CO3]

(xx) The total number of memory accesses involved when STA 58EBH instruction is executed is

a) 4 b) 6 c) 1 d) 2 [CO2]

Kushal Roy

Signature of the Paper Setter/Moderator

Answer Key:

Group – A

1. (i) a (ii) c (iii) c (iv) b (v) c (vi) c (vii) a (viii) b (ix) b (x) d (xi) d (xii) a (xiii) c (xiv) c (xv) c (xvi) d (xvii) a (xviii) a (xix) c (xx) c (xxi) d (xxii) c (xxiii) c (xxiv) d (xxv) d (xxvi) a (xxvii) a (xxviii) b (xxix) a (xxx) b

Group – B

2. (i) a (ii) c (iii) c (iv) d (v) d (vi) c (vii) a (viii) b (ix) a (x) c (xi) d (xii) b (xiii) a (xiv) b (xv) d (xvi) a (xvii) a (xviii) c (xix) b (xx) a