



HALDIA INSTITUTE OF TECHNOLOGY

(AN AUTONOMOUS INSTITUTION UNDER MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL)

Paper Code: ESC 301

Paper Name: Digital Logic Design

Time Allotted: 3 Hours

Full Marks: 70

The figures in the margin indicate full marks

Candidates are required to give their answers in their own words as far as practicable

Group – A

(Multiple Choice Type Questions)

Choose the correct alternatives from the followings:

15 x 1 = 15

1. (i) Which of the following codes is a sequential code?

- a) 8421 code b) 2421 code c) 5421 code d) 2441 code [CO1]

(ii) How many bits are needed to store one BCD digit?

- a) 2 bits b) 4 bits c) 3 bits d) 1 bit [CO1]

(iii) Which gate is called the anti – coincidence and coincidence gate respectively?

- a) XNOR and XOR b) AND and OR c) OR and AND d) XOR and XNOR [CO1], [CO2]

(iv) 2's complement of 1011011 is

- a) 0100011 b) 0110101 c) 0100011 d) 0100101 [CO1]

(v) The ASCII code is basically

- a) 5 bit code b) 6 bit code c) 7 bit code d) 4 bit code [CO1]

(vi) The range of values that can be represented with 8 bit in 2's complement form is

- a) 0 to +128 b) +256 to -256 c) -128 to +128 d) +127 to -128 [CO1]

(vii) Which of the following gives the correct number of multiplexers required to build a 32 x 1 multiplexer?

- a) Two 16 x 1 mux b) Three 8 x 1 mux c) Two 8 x 1 mux d) Three 16 x 1 mux [CO3]

(viii) The minimum number of 2-input NAND gates are required to realize a half adder is

- a) 8 b) 5 c) 6 d) 4 [CO1], [CO2], [CO3]

(ix) In order to design 5 bit comparator, how many output(s) is/are needed?

- a) 1 b) 2 c) 3 d) 4 [CO3]

(x) How many 3-line-to-8-line decoders are required for a 5-to-32 decoder?

- a) 4 b) 1 c) 8 d) 2 [CO3]

(xi) Invalid BCD can be made to valid BCD by adding with

- a) 0101 b) 0110 c) 0111 d) 1001 [CO3]

(xii) A digital circuit that can store only one bit is a

- a) Register b) NOR gate c) Flip-flop d) XOR gate [CO5]

(xiii) In the toggle mode, a JK flip-flop has

- a) J = 0, K = 1 b) J = 1, K = 1 c) J = 0, K = 0 d) J = 1, K = 0 [CO4]

(xiv) The sequential circuit is also called _____
a) Flip-flop b) Latch c) Strobe d) Adder [CO4]

(xv) Recommended fan-out for TTL gate is _____
a) 10 b) 4 c) 20 d) 50 [CO6]

Group – B

(Short Answer Type Questions)

Attempt any three from the followings: **3 x 5 = 15**

2. (i) What is a Venn diagram? [CO1]

(ii) Prove that the De Morgan's Theorem. [CO1] [CO2] 2+3

3. What is ASCII Code? What is the full form of ASCII & EBCDIC? Give one example for each case. [CO1] 3+2

4. Design Adder/Subtractor composite unit using 4-bit binary full adder and necessary gates. 5
[CO1]

5. Perform the conversion from the J-K flip-flop to D flip-flop. [CO3] 5

6. (i) What is the need A/D and D/A converters in controlling a process? [CO6]

(ii) A DAC has a full scale analog output of 10 V and accepts 6 bits as input. Find the voltage corresponding to each analog step. [CO6] 3+2

Group – C

(Long Answer Type Questions)

Attempt any four from the followings: **4 x 10 = 40**

7. (i) Simplify the following Boolean expressions and implement using basic gates. [CO2]

$$Y = ABC + \bar{A}\bar{B}C + AB\bar{C}$$

$$Y = \overline{(AB + \bar{C})}(\bar{A} + \bar{B} + C)$$

(ii) Express the given Boolean function in sum of minterms: $F = A + \bar{B}C$ and implement the function using NAND gates. [CO2] 6+4

8. (i) Minimize the logic function using K-Map and implement by logic gates. [CO2]

$$F(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 8, 10, 12, 14, 15)$$

(ii) Minimize the logic function using K-Map and implement by logic gates. [CO2]

$$F(A, B, C, D) = \sum m(0, 1, 2, 8, 9, 10, 14) + \sum d(6, 7, 12, 15)$$
5+5

9. (i) Design 4-Bit Binary Parallel Adder circuit using 1-Bit Adder. [CO3]

(ii) Design BCD Adder circuit using 4-Bit Binary Parallel Adder and explain the design with example. [CO3] 3+7

10. (i) What is Decoder? [CO3]

(ii) Design a 4-line to 16-line decoder using 2-line to 4-line decoder. [CO3]

(iii) Design full-adder and full-subtractor using decoder. [CO3] 2+4+4

11. (i) What is the difference between a Flip-Flop and Latch? [CO4]

(ii) Derive the Boolean expression for the characteristic equation of J-K flip flop. [CO4]

(iii) Draw the circuit diagram and output waveform of a MOD-8 ripple counter. [CO5] 3+2+5

12. (i) Write the characteristics of digital IC. [CO6]

(ii) Comprising of the different TTL series. [CO6]

(iii) Define the following parameters of logic families [CO6]

a) Noise margin b) Propagation Delay c) Power Dissipation d) Fan-out 2+4+4